

Simulyzer-RT DIO-2 Card



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Safety instructions

To avoid damages to persons and devices the following safety instructions have to be noticed!

- Only qualified personnel are allowed to handle this device!
- Before any handling within the device the current supply has to be switched off!
- During operation the device have to be positioned, that enough air condition is supplied and no small parts can get into the ventilation slots.
- In case of any trouble the system has to be switched de-energized!
- The declared environmental conditions and max. voltage ranges have to be observed!
- To warranty the device remove all dust and dirt in periodically intervals.
- Make sure that the ventilation slots are unobstructed!

Intended use:

The Simulyzer RT DIO-2 card is engineered for measurement and analysis of sensors of a RT proofing system. The field of function of the DIO-2 card is the digital data transfer within the test system (see applications).

- The device is only permitted to use for the intended use.
Any other use results the deletion of the guarantee!

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The Simulyzer-RT DIO-2 board is a further development of the Simulyzer-RT DIO-1 board in the areas:

- Significantly higher FPGA size for the implementation of more complex processes.
- Significantly higher computing power for measured value preprocessing;
DIO-1: 100,000 signal values/s
DIO-2: 4.000.000 signal values/s

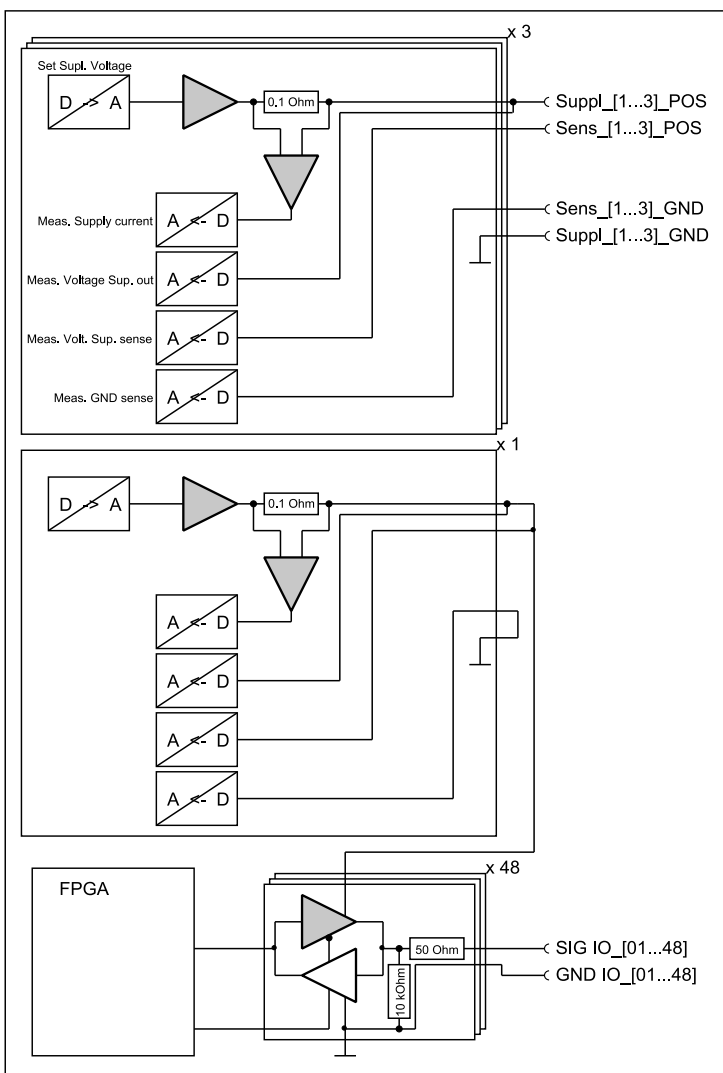
1. Technical data

- Current consumption: 12V / 0,8 A (without external consumers)
- Operating temperature: 0°C ... 40°C
- Rel. Humidity: Max. 85% not condensed
- Weight: 190g
- Dimensions: Single Eurocard, 4 U

Test conditions: Environmental temperature 20°C to 26°C

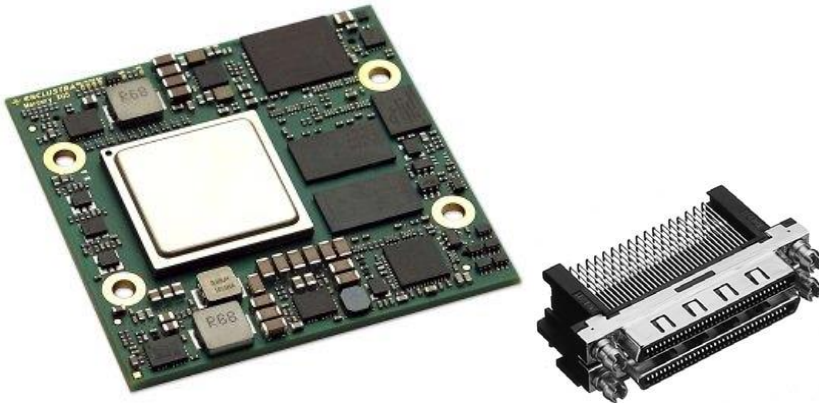
Num	Evaluation	Symbol	typ.	min.	max.	description
1	Permitted voltage range	U_{supp}	12V	11.4V	12.6V	
2	Current consumption	I_{supp}	650mA	-	800mA	Without sensor supply

2. Block diagram



3. Connectors:

- For SPI, FAST-SO
- Connectors to bus:
 - 1 PCIe Lane to CPU-1
 - Power supply I2C
 - Parallel to all cards for synchronization
- Connectors frontside: HDRA-E68W1LFDTC „Dual Stacking Connectors“ with dig IO + Sensor Power

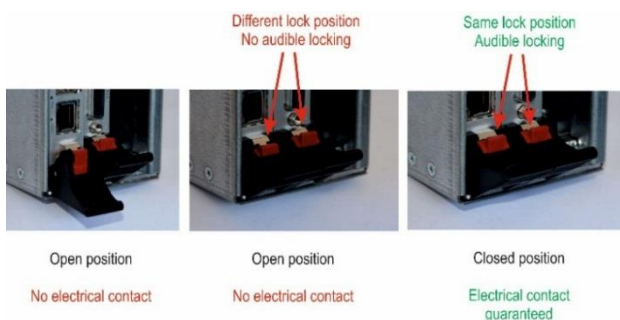


4. Interfaces and FPGA:

- Xilinx® Zynq® UltraScale+ MPSoC Modules for the realization of protocols. ARM® dual-/quad-core Cortex™-A53 (64 bit, up to 1500 MHz)
- 8 x SPI (MISO, MOSI, CS, CLK) + 16 Reserve DIG IO => 48 Pins
- 16xSPI (16xMISO, 16xMOSI, 8xCS, 8xCLK)/ 48 Pins
- With the 16 reserve IO, 4 x Fast-SO can be realized, among other things.
- All DIG IOs bidirectional, level adjustable from 1.2V to 5.5V operation; max. 20MHz
- 3x adjustable PU outputs, 0.5V to 6.0V, +/- 0.1% of full scale for external supply of the sensors, current limitation 0..1000mA, +/- 0.1%.
1x adjustable PU output, 0.5V to 6.0V, +/- 0.1% of full scale, current limitation 0..1000mA +/- 0.1%.
- for internal drivers (+ external)50 Ohm or 100 Ohm Impedanz Adaptation for coaxial or twisted pair lines
- Back measurement of the 4 PU voltages and the 4 currents. Accuracy: +/- 0.1% of the full scale value

5. Handling card/chassis

Pay attention that the ejection lever of the plug-in card is arrested correctly. Only the correct position guarantees a justly connection of the bus system and the power supply!



Note

The forcible insertion of the card with displaced HF-sealing spring will damage them. As a result of that HF energy emission will be increased!

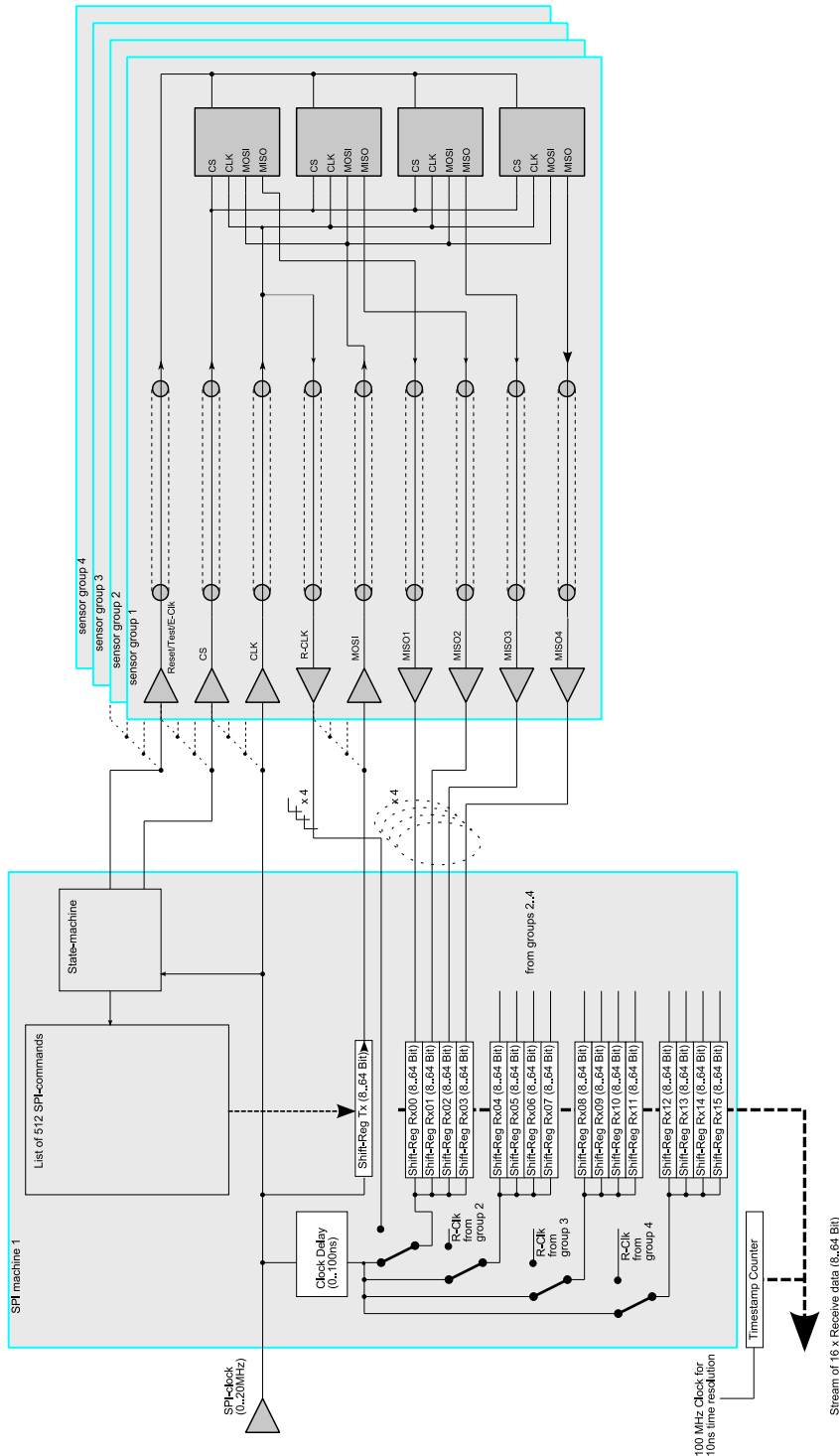
Only with intact HF-sealing spring we guarantee that the whole system conforms to the EMC guidelines.

HF-sealing spring

6. Applications – Working modes

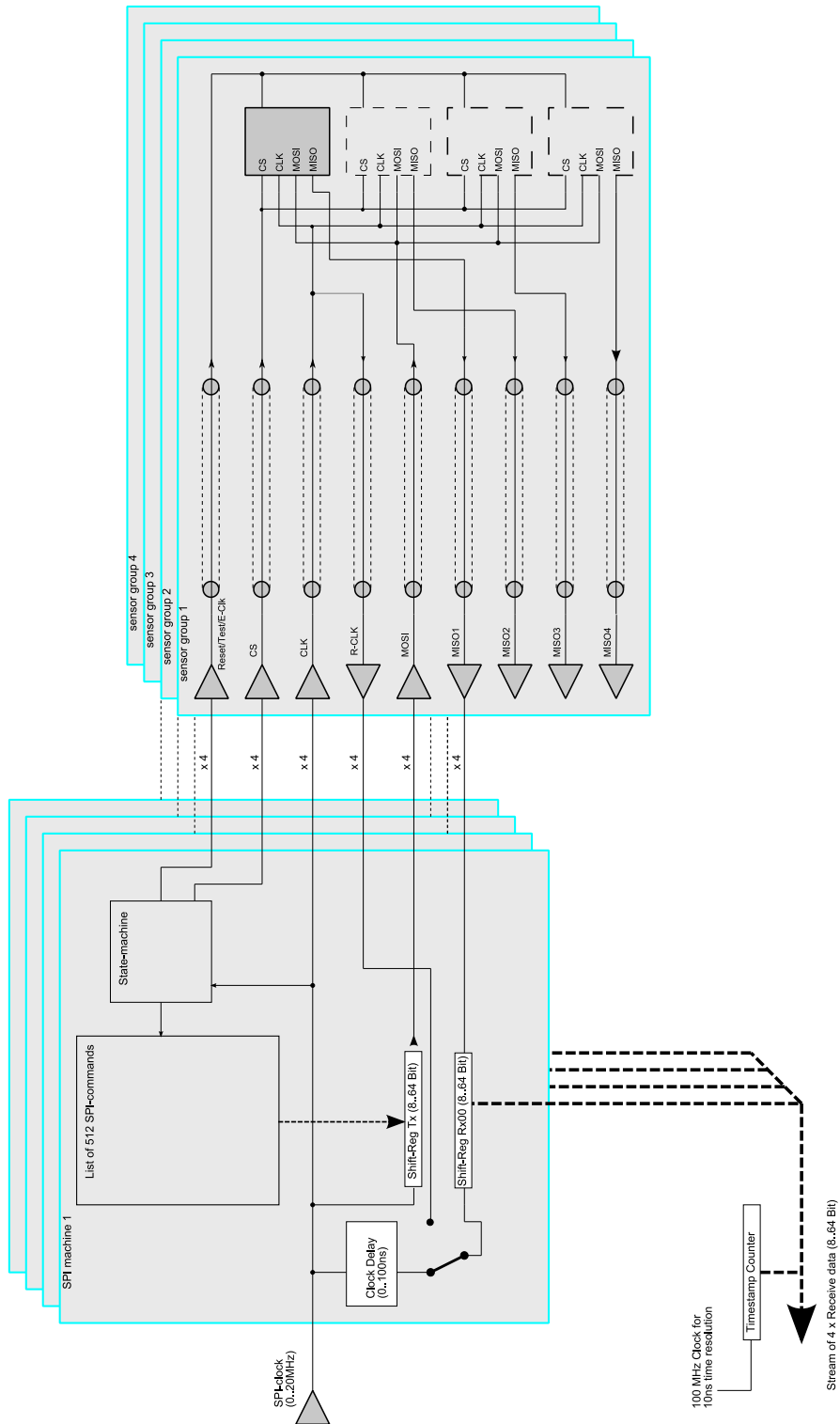
6.1. 16-times highspeed measurement application

For the application of a 16-fold-parall measurement technique a SPI machine is implemented in the FPGA, which controls the slave-in of 16 sensors together from a transmit shift register. Chip select, clock and possibly reset/test are also controlled together. Individually implemented are the 16 slave-out lines, which go to 16 receive shift registers. The commands go absolutely synchronously to all 16 sensors, the answers are received individually.



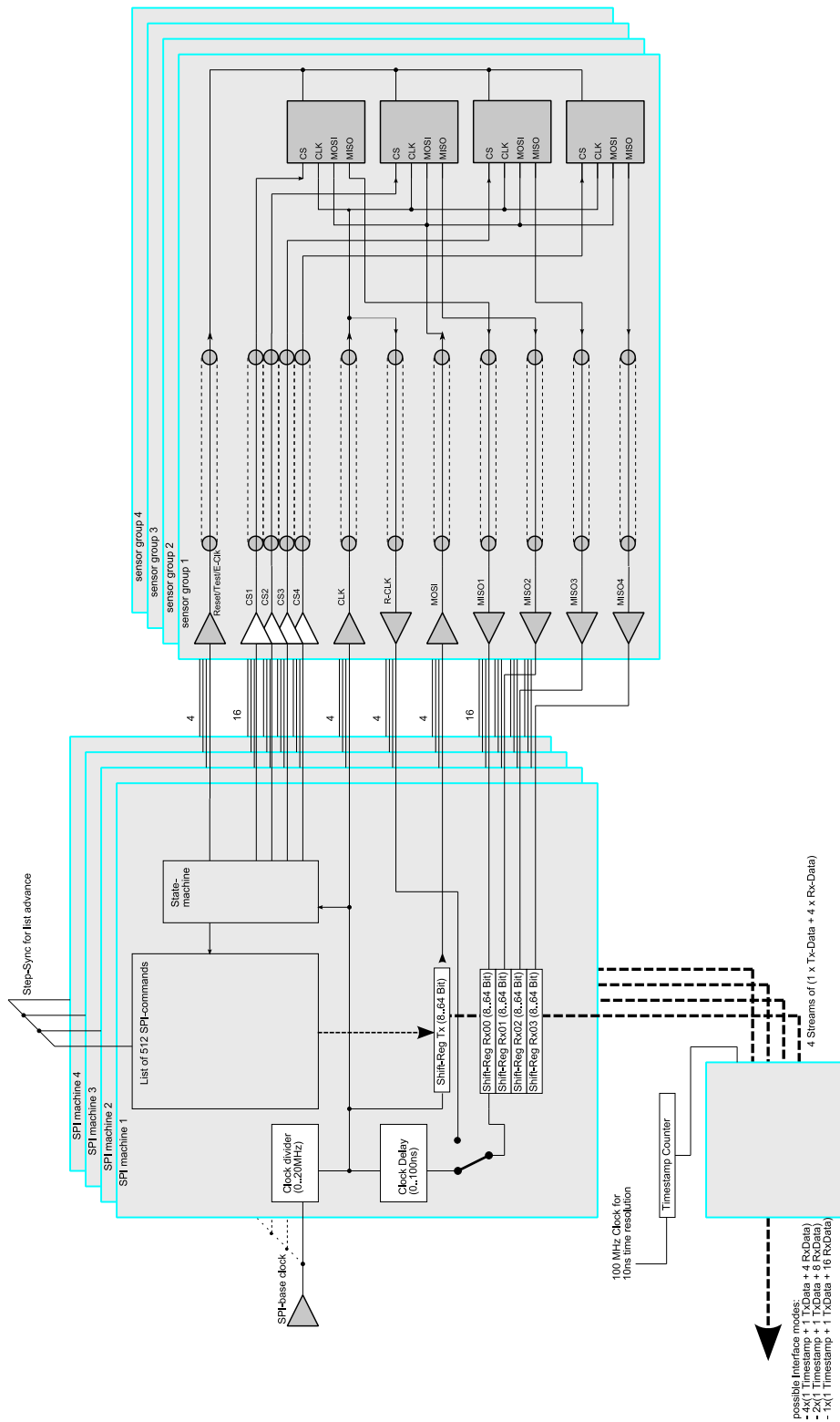
6.2. 4-times comparison application

4 SPI machines each with one own sending- and receiving shift register.
 Each SPI machine serves the first sensor of each 4 times group.
 The rest of the three sensors of each group stay unpopulated.



6.3. 16-times high-speed measurement application with different sensors

At the FPGA four SPI machines are implemented, which each controls the *Slave-In* of 4 sensors of a group in common out of its 4 sending shift register. *Clock* and optionally *Reset/Test* are also controlled in common. Individually executed are the 16 *Slave-Out* lines, which are connected to the 4 receiving shift register of the 4 groups.



7. Measurement accuracy

7.1. Time base

Test conditions: Environmental temperature 20°C to 26°C						
Num	Evaluation	Symbol	Type	Max	Unit	Comment
1	Accuracy time base	$\Delta f/f$	± 30	± 50	ppm	-
2	Aging of time base	$\Delta f/f_A$	± 5		ppm/year	-
3	Temperature drift of time base	$\Delta f/f_T$	± 0.3	± 0.7	ppm/°C	-

7.2. Measurement of the supply voltage

Test conditions: Environmental temperature 20°C to 26°C						
Num	Evaluation	Symbol	Type	Max	Unit	Comment
4	Accuracy of the measured voltage	U_{mea}	± 0.3	± 0.4	% of scfin. 7.5V	Range 0.5V .. 6.0V
5	Aging of the measured voltage	U_{A-meas}		± 0.1	%/year	Range 0.5V .. 6.0V
6	Resolution of the measured voltages		16		Bit	0.. 65535
			0.1144409		mV/LSB	

7.3. Measurement of the supply currents

Test conditions: Environmental temperature 20°C to 26°C						
Num	Evaluation	Symbol	Type	Max	Unit	Comment
7	Accuracy of the measured current	I_{mea}	± 0.3	± 0.4	% of scfin. 1000mA	Range 2mA .. 900mA
8	Aging of the measured current	I_{A-meas}		± 0.1	% of scfin. 1000mA / year	Range 2mA .. 900mA
9	Resolution of the measured current		16		Bit	0.. 65535
			15,2587891		μA/LSB	

7.4. Generation of the voltages

Test conditions: Environmental temperature 20°C to 26°C						
Num	Evaluation	Symbol	Type	Max	Unit	Comment
10	Accuracy of the created current	U_{mea}	± 0.3	± 0.4	% of scfin. 6.3V	Range 0.5V .. 6.0V
11	Aging of the created current	U_{mea}		± 0.1	% of scfin 6.3V / year	Range 0.5V .. 6.0V
12	Resolution of the created current		16		Bit	0.. 65535
			0,096130371		mV/LSB	

8. Connection diagram X10/X11

Pin	Paar	Belegung Stecker 1 (Rand)
1	1	GND
35	1	Sig_IO 01
2	2	GND
36	2	Sig_IO 02
3	3	GND
37	3	Sig_IO 03
4	4	GND
38	4	Sig_IO 04
5	5	GND
39	5	Sig_IO 05
6	6	GND
40	6	Sig_IO 06
7	7	GND
41	7	Sig_IO 07
8	8	GND
42	8	Sig_IO 08
9	9	GND
43	9	Sig_IO 09
10	10	GND
44	10	Sig_IO 10
11	11	GND
45	11	Sig_IO 11
12	12	GND
46	12	Sig_IO 12
13	13	GND
47	13	Sig_IO 13
14	14	GND
48	14	Sig_IO 14
15	15	GND
49	15	Sig_IO 15
16	16	GND
50	16	Sig_IO 16
17	17	GND
51	17	Sig_IO 17
18	18	GND
52	18	Sig_IO 18
19	19	GND
53	19	Sig_IO 19
20	20	GND
54	20	Sig_IO 20
21	21	GND
55	21	Sig_IO 21
22	22	GND
56	22	Sig_IO 22
23	23	GND
57	23	Sig_IO 23
24	24	GND
58	24	Sig_IO 24
25	25	GND
59	25	+VCC1
26	26	GND
60	26	+VCC1
27	27	GND
61	27	+VCC1
28	28	GND
62	28	Sense VCC1
29	29	GND
63	29	Sense GND1
30	30	GND
64	30	+VCC2
31	31	GND
65	31	+VCC2
32	32	GND
66	32	+VCC2
33	33	GND
67	33	Sense VCC2
34	34	GND
68	34	Sense GND2

Pin	Paar	Belegung Stecker 2 (innen)
1	1	GND
35	1	Sig_IO 25
2	2	GND
36	2	Sig_IO 26
3	3	GND
37	3	Sig_IO 27
4	4	GND
38	4	Sig_IO 28
5	5	GND
39	5	Sig_IO 29
6	6	GND
40	6	Sig_IO 30
7	7	GND
41	7	Sig_IO 31
8	8	GND
42	8	Sig_IO 32
9	9	GND
43	9	Sig_IO 33
10	10	GND
44	10	Sig_IO 34
11	11	GND
45	11	Sig_IO 35
12	12	GND
46	12	Sig_IO 36
13	13	GND
47	13	Sig_IO 37
14	14	GND
48	14	Sig_IO 38
15	15	GND
49	15	Sig_IO 39
16	16	GND
50	16	Sig_IO 40
17	17	GND
51	17	Sig_IO 41
18	18	GND
52	18	Sig_IO 42
19	19	GND
53	19	Sig_IO 43
20	20	GND
54	20	Sig_IO 44
21	21	GND
55	21	Sig_IO 45
22	22	GND
56	22	Sig_IO 46
23	23	GND
57	23	Sig_IO 47
24	24	GND
58	24	Sig_IO 48
25	25	GND
59	25	+VCC3
26	26	GND
60	26	+VCC3
27	27	GND
61	27	+VCC3
28	28	GND
62	28	Sense VCC3
29	29	GND
63	29	Sense GND3
30	30	GND
64	30	+VCC4
31	31	GND
65	31	+VCC4
32	32	GND
66	32	+VCC4
33	33	GND
67	33	GND
34	34	GND
68	34	GND

9. Connection diagram X10/X11 as a 4x4 SPI Master Machine

Pin	Paar	Belegung Stecker 1 (Rand)
1	1	GND
35		CLK_G1
2	2	GND
36		R_CLK_G1
3	3	GND
37		MOSI_G1
4	4	GND
38		RES_TEST_E_G1
5	5	GND
39		CS_G1_S1
6	6	GND
40		CS_G1_S2
7	7	GND
41		CS_G1_S3
8	8	GND
42		CS_G1_S4
9	9	GND
43		MISO_G1_S1
10	10	GND
44		MISO_G1_S2
11	11	GND
45		MISO_G1_S3
12	12	GND
46		MISO_G1_S4
13	13	GND
47		CLK_G2
14	14	GND
48		R_CLK_G2
15	15	GND
49		MOSI_G2
16	16	GND
50		RES_TEST_E_G2
17	17	GND
51		CS_G2_S1
18	18	GND
52		CS_G2_S2
19	19	GND
53		CS_G2_S3
20	20	GND
54		CS_G2_S4
21	21	GND
55		MISO_G2_S1
22	22	GND
56		MISO_G2_S2
23	23	GND
57		MISO_G2_S3
24	24	GND
58		MISO_G2_S4
25	25	GND
59		+VCC1
26	26	GND
60		+VCC1
27	27	GND
61		+VCC1
28	28	GND
62		Sense VCC1
29	29	GND
63		Sense GND1
30	30	GND
64		+VCC2
31	31	GND
65		+VCC2
32	32	GND
66		+VCC2
33	33	GND
67		Sense VCC2
34	34	GND
68		Sense GND2

Pin	Paar	Belegung Stecker 2 (innen)
1	1	GND
35		CLK_G3
2	2	GND
36		R_CLK_G3
3	3	GND
37		MOSI_G3
4	4	GND
38		RES_TEST_E_G3
5	5	GND
39		CS_G3_S1
6	6	GND
40		CS_G3_S2
7	7	GND
41		CS_G3_S3
8	8	GND
42		CS_G3_S4
9	9	GND
43		MISO_G3_S1
10	10	GND
44		MISO_G3_S2
11	11	GND
45		MISO_G3_S3
12	12	GND
46		MISO_G3_S4
13	13	GND
47		CLK_G4
14	14	GND
48		R_CLK_G4
15	15	GND
49		MOSI_G4
16	16	GND
50		RES_TEST_E_G4
17	17	GND
51		CS_G4_S1
18	18	GND
52		CS_G4_S2
19	19	GND
53		CS_G4_S3
20	20	GND
54		CS_G4_S4
21	21	GND
55		MISO_G4_S1
22	22	GND
56		MISO_G4_S2
23	23	GND
57		MISO_G4_S3
24	24	GND
58		MISO_G4_S4
25	25	GND
59		+VCC3
26	26	GND
60		+VCC3
27	27	GND
61		+VCC3
28	28	GND
62		Sense VCC3
29	29	GND
63		Sense GND3
30	30	GND
64		+VCC4
31	31	GND
65		+VCC4
32	32	GND
66		+VCC4
33	33	GND
67		GND
34	34	GND
68		GND